Pixel Concept for CDF/D0 in Run IIb

- Pixels are feasible for Run IIb
- Pixel R&D at FNAL
- Pixels have advantages
  - r-ϕ and r-z resolution
  - radiation hardness
  - large S/N and high efficiency
  - pattern recognition
- Pixels have disadvantages
  - additional material
  - complex system
- Strawperson designs and options

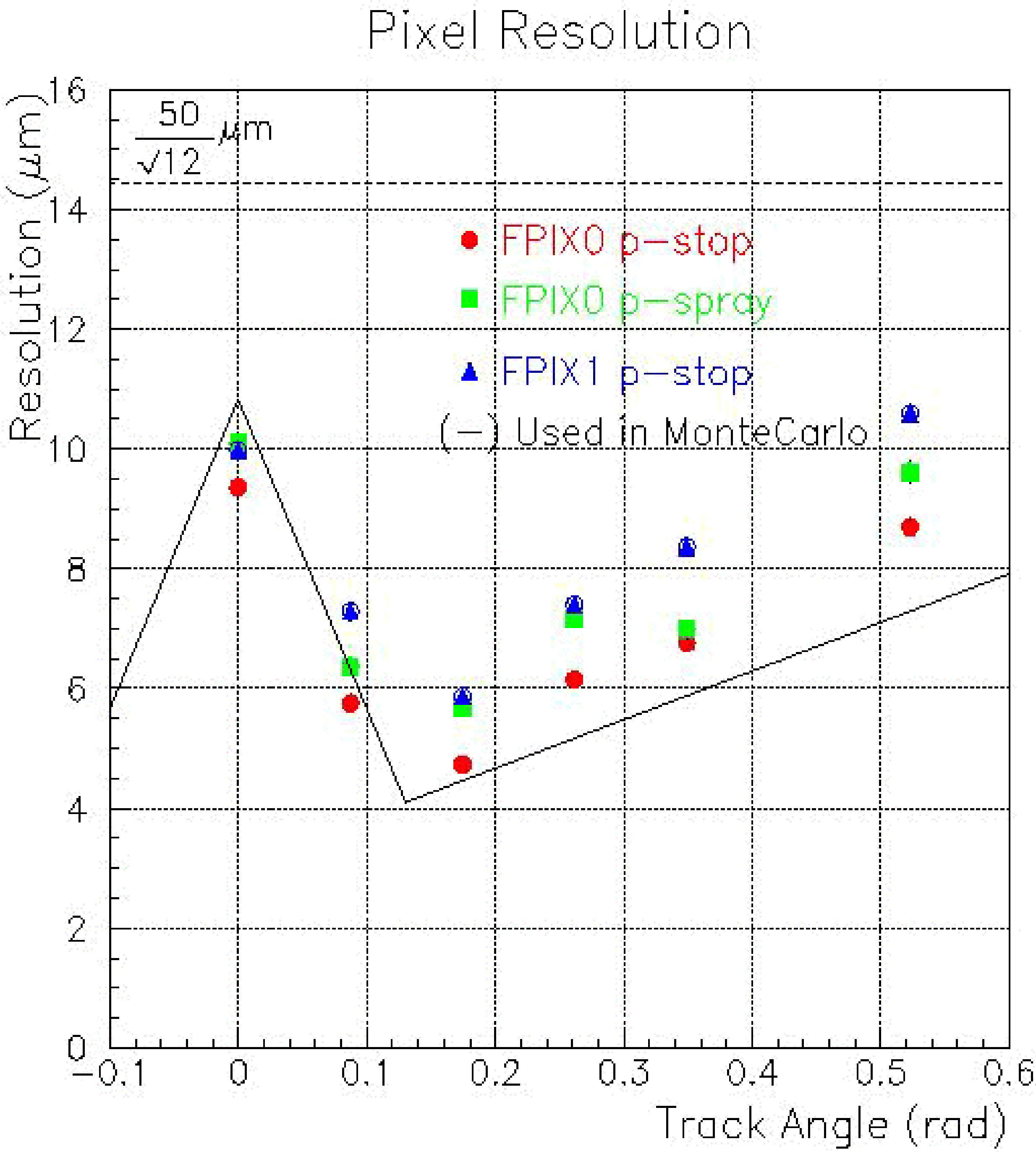
Pixels are feasible for Run IIb

- Use ATLAS style sensor design
- Use FPIX style chip developed at FNAL (“the BTeV chip”)
- Use DAQ components that can utilize CDF/D0 modules (VRB)
- R&D on system design (mechanical, cables, etc)
- Test beam demonstrated

Pixel test beam results

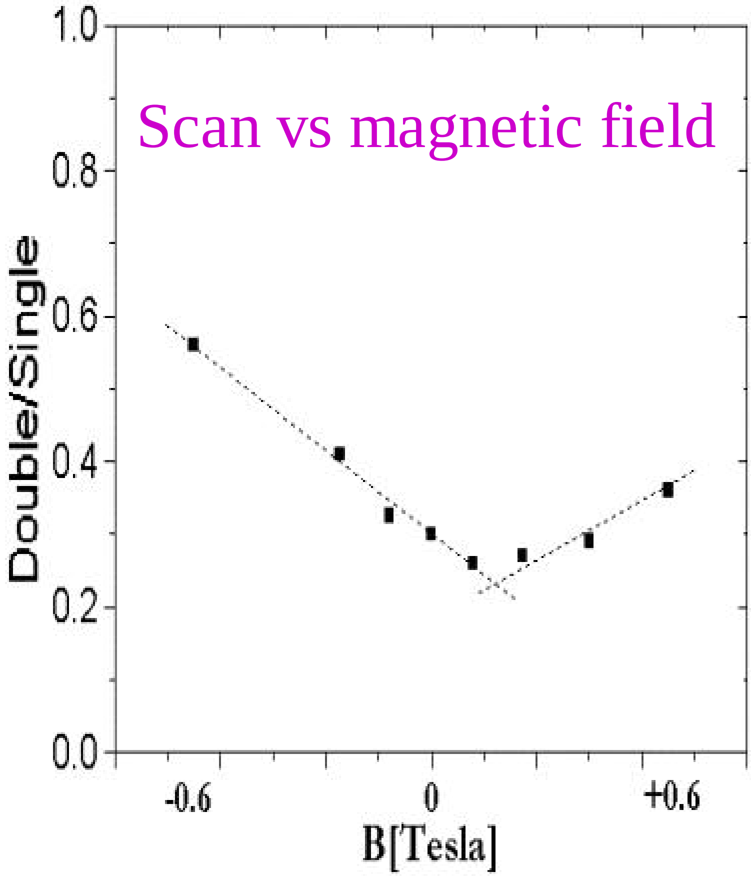
- 5 pixel detectors characterized
- scan vs angle, bias voltage, threshold
- resolution in B field (0.6 T)
- target data

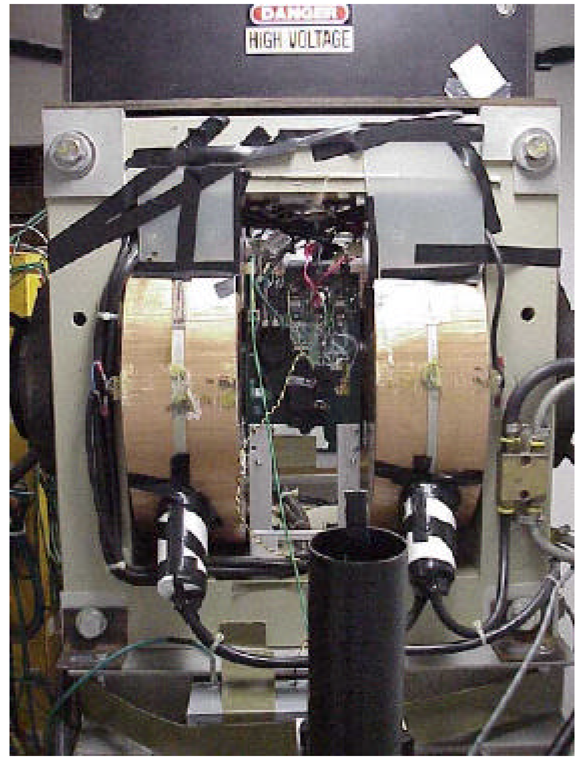
Scan vs Track Angle

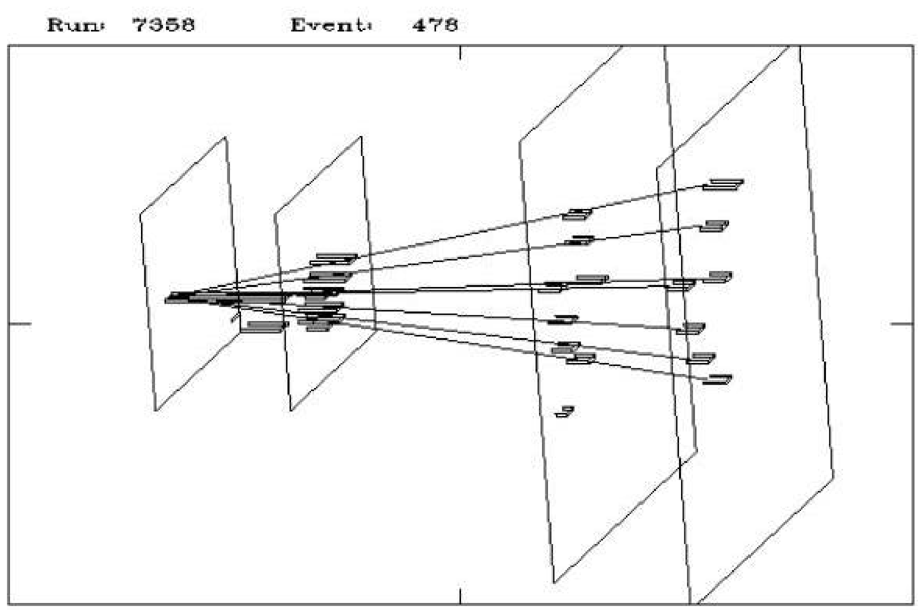


Preliminary, see also http://www-rhvd.fnal.gov/

Other results





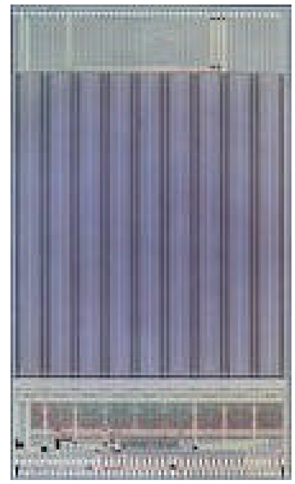


Target data with 4 pixel planes.

Pixel R&D at Fermilab

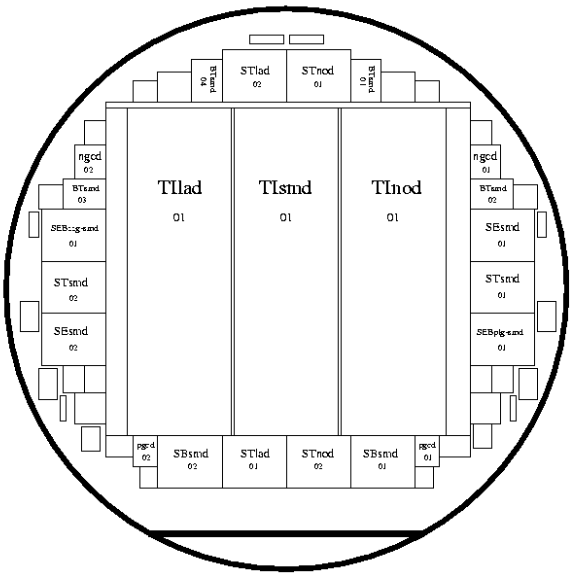
- Rad hard vertex group at FNAL
- BTeV is first customer, but resources are available to any Fermilab experiment
- FPIX chip
  - FPIX0 (1998) 0.8 μm HP CMOS
  - FPIX1 (1999) 0.5 μm HP CMOS
  - FPIX2 (2000) 0.25 μm rad hard
    - pre-FPIX2 in hand
    - April radiation tests to 30+ Mrads
- ATLAS-style sensors
- Mechanical Support
- DAQ

FPIX1 chip



- 160 pixels x 18 columns matching 50μ x 400μ pixels
- Designed for 132 ns
- Pixel cell: charge sensitive amplifier, 2-bit flash ADC with discriminator
- Chip control logic
- End-of-column logic: controls the column of cells and holds the timestamp for hits

ATLAS sensors

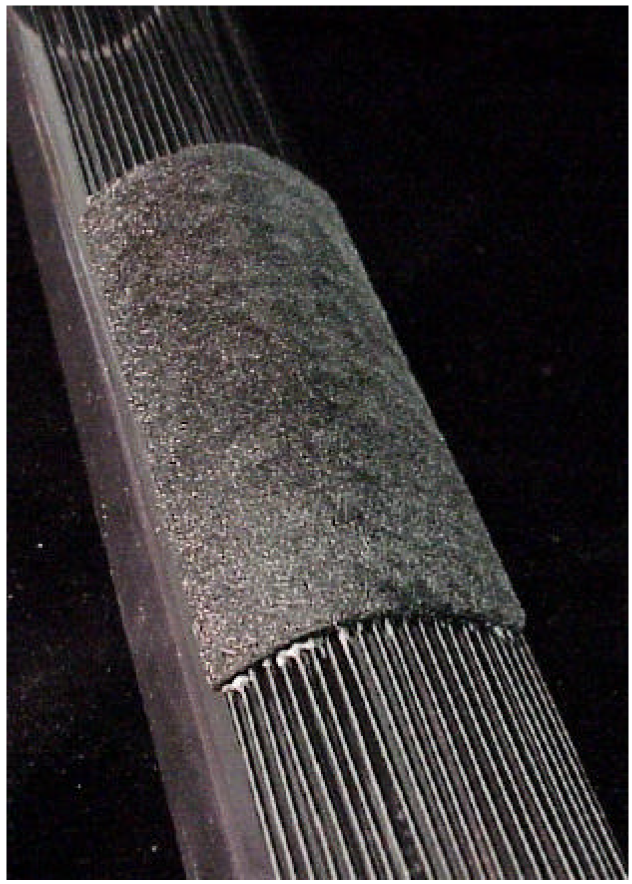


4 inch wafers
3 “tiles” = 47232 pixels
16 units each with 2880 channels read out with a readout chip
Also, single chip sensors and test structures
BTeV likely to use a single row of readout chips per sensor

- Advanced design -- out for bids or nearly out for bids
- n+ pixels on n bulk with p-spray isolation on the n side
- guard rings on the p side
- Performance out to fluence=10^15 / cm^2
- Bias up to 600V or more

Mechanical support

- CDF/D0 specific R&D would be needed
- Fuzzy carbon supports look promising
- Be support structures can also be used
- Cooling incorporated into support



Pixel DAQ

- CDF/D0 specific R&D would be needed. FPIX "core" is near final. The "periphery" is flexible and experiment dependent.
- Flex circuit with bonds to FPIX chips looks promising
- Data serialized and transmitted via optical fiber (VCSELs) or LVDS drivers over copper
- Deep memory module that sorts hits w/time stamp to hits for events

Pixel Advantages

- Radiation hardness
  - expected to 10^15 / cm^2 (~40 Mrad); last replacement
- Position resolution
  - between 4-10 μm residuals
  - can design to trade off r-φ and r-z
- S/N
  - noise typically 100 e-
  - S/N remains good v dose
- Pattern recognition
  - 3d space points
- Studies needed to quantify advantages in *b*-tagging, etc.

Pixel disadvantages

- Amount of material
  - material needed for readout and cooling in the active volume
  - 1.5 - 2.5% of a radiation length for a layer of pixels
- Heat dissipation
- Complexity
  - judgement

Proposal to CDF for consideration

- **Replace Layer00 with single layer of pixels -- best choice for a position measurement close to the beam with high S/N after very high radiation.**
  - Minimize risk by pursuing both single-sided silicon and pixel options (at least initially)
  - Option to re-use SVXII or use new single-sided strips
  - Scale is about 10% of the BTeV pixel system. Estimate $1M.

Status

- R&D continues
  - 5-chip module shows good noise
  - BTeV periphery under design
- Initial CDF effort
  - **focus on single-sided silicon**
  - begin pixel conceptual design
  - expected occupancy drives DAQ
  - email distribution list/web page
  - performance simulations
- Best detector with high luminosity for the best chance of a Run II discovery.